UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,890	04/02/2001	Kevin J McGrath	5500-54701	1609

7590 10/21/2004

Lawrence J. Merkel
Conley, Rose, & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,890	MCGRATH ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36 and 49-51* is/are rejected.

7)☒ Claim(s) *37-48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *21 July 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 and new claims 34-51 have been considered. Claims 1-7, 22-25, and 32-33 have been amended as per Applicant's request. New claims 34-51 have been added as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as filed on 21 July 2004.

Claim Objections

3. Claims 37-48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

4. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

5. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

6. Claims 23-24 and 32-33 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 17-18 and 21-22 respectively of copending Application No. 09/483,101. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

8. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

9. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-6 and 22 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 and 10 of copending Application No. 09/483,101. Although the conflicting claims are not identical, they are not patentably distinct from each other because the additional limitation in the current application, "a processor configured to process an instruction using said default address size" is inherent to the claims in 09/483,101. When establishing an address size, it is inherent that the system would process instructions using the address size. Claims of application number 09/483,101 contain every element of claims 1-6 and 22 of the instant application and as such anticipates claims 1-6 and 22 of the instant application.

11. "A later patent claim is not patentable distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fred. Cir. 1998) (affirming a holding of

obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus)." ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

12. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1, 14-20, 23, 34-35, and 49-51 are rejected under 35 U.S.C. 102(b) as being taught by James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley).

15. Referring to claim 1, Turley has taught an apparatus comprising:

a. A first storage location configured to store a segment selector (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4) identifying a segment descriptor (Turley Page 63, Paragraph 4) including a first operating mode indication, a second operating mode indication (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table), and one or more bits identifying a segment described by said segment descriptor as a code

segment (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57);

b. A second storage location configured to store an enable indication (Turley Page 26, Control Register 0, element PE), wherein said enable indication, said first operating mode indication, and said second operating mode indication are indicative of a default address size (Turley Page 48, Paragraph 3 and Page 178, Paragraphs 2-3); and

c. A processor configured to process an instruction using said default address size (Turley Page 52, Paragraph 2).

16. Referring to claim 34, Turley has taught a computer readable medium storing a plurality of native instructions executable directly on a processor (Turley pages 283-286), wherein the plurality of native instructions comprise native instructions which, when executed, perform one or more operations defined for a non-native instruction using a default address size (Turley pages 283-286), the default address size determined in response to an enable indication in a first storage location (Turley Page 176, Paragraph 1 and Page 178, Paragraph 2-3), a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table), wherein said segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57).

17. Referring to claims 14-19 and 49-51, Turley has taught

a. Wherein said first storage location is a memory location (Applicant's claims 14 and 49) (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4), general purpose register within said processor (Applicant's claims 15 and 50) (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4), or a special purpose register within said processor (Applicant's claims 16 and 51) (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4). In regards to Turley, the segment selector is stored in a register designed to hold the segment selector data, which means it is a type special purpose register. Also, a memory location, by definition, is a specified location within a computer storage device and a register is a computer storage device, which means that the register holding the segment selector is a type of memory location. A general purpose register, by definition, is a register that can be used for different purposes, including as a special handler of data, which means that a register which handles special data, such as a segment register, is a type of general purpose register. For more information regarding these definitions, please see Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition pages 256, 377, 526, and 592.

b. Wherein said second storage location is a memory location (Applicant's claim 17) (Turley Page 26, Control Register 0, element PE), general purpose register within said processor (Applicant's claim 18) (Turley Page 26, Control Register 0, element PE), or a special purpose register within said processor (Applicant's claim 19) (Turley Page 26, Control Register 0,

element PE). In regards to Turley, the enable indication is stored in a register designed to hold the enable indication data, which means it is a type special purpose register. Also, a memory location, by definition, is a specified location within a computer storage device and a register is a computer storage device, which means that the register holding the segment selector is a type of memory location. A general purpose register, by definition, is a register that can be used for different purposes, including as a special handler of data, which means that a register which handles special data, such as a segment register, is a type of general purpose register. For more information regarding these definitions, please see Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition pages 256, 377, 526, and 592.

18. Referring to claim 20, Turley has taught wherein said processor is configured to process said instruction by executing interpreter software which emulates said instruction (Turley pages 283-286).

19. Referring to claim 23, Turley has taught a method comprising:

a. Determining a default address size (Turley Page 48, Paragraph 3 and Page 178, Paragraphs 2-3) in response an enable indication in a first storage location (Turley Page 176, Paragraph 1 and Page 178, Paragraph 2-3), a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor (Turley Page 49, Table: A segment descriptor; Pages 47-48, Paragraphs 5 to 2; Page 50, Figure 2-2; Page 51-52; Page 53, Paragraph 3; and Page 54, Table),

wherein said segment descriptor further includes one or more bits identify a segment described by said segment descriptor as a code segment (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57)

b. Generating addresses in response to said default address size (Turley Page 52, Paragraph 2).

20. Referring to claim 35, Turley has taught wherein the native instructions emulate the non-native instruction (Turley pages 283-286).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80386 Programming Techniques (herein referred to as Turley) in view of Schrofer, U.S. Patent Number 4,682,284 (herein referred to as Schrofer).

23. Referring to claim 26, Turley has taught

a. Wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table having a plurality of entries (Applicant's claim 26) (Turley page 59-61);

b. A second segment descriptor of said plurality of segment descriptors from said segment descriptor table (Applicant's claim 26) (Turley page 59-61).

24. Turley has not taught wherein said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor (Applicant's claim 26). Schrofer has taught wherein said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor (Applicant's claim 26) (Schrofer column 8, lines 27-42). In regards to Schrofer, he has illustrated the use and need for the use of multiple storage locations for larger data words. A person of ordinary skill in the art at the time the invention was made would have recognized that multiple entries are needed to store larger data words, thereby increasing the accuracy and variety of data the system uses. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiple storage locations of Schrofer in the device of Turley to increase the accuracy and variety of data used in the system.

25. Referring to claim 27, Turley has taught a call gate descriptor (Turley page 478).

26. Referring to claim 28, Turley has taught an interrupt gate descriptor (Turley 479).

27. Referring to claim 29, Turley has taught a trap gate descriptor (Turley page 479).

28. Referring to claim 30, Turley has taught a task state segment descriptor (Turley page 479).

29. Referring to claim 31, Turley has taught a local descriptor table descriptor (Turley page 480). In regards to Turley, an LDT is a local descriptor table.

30. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80386 Programming Techniques (herein referred to as Turley) in

view of Park, U.S. Patent Number 6,021,484 (herein referred to as Park). Turley has not taught wherein said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed by said processor. Park has taught wherein said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed by said processor (Park column 1, line 57 to column 2, line 8 and column 2, lines 48-59). In regards to Park, whether translating instructions is conducted in hardware or software, it does not matter since they are functionally equivalent. A person of ordinary skill in the art at the time the invention was made would have recognized that translation software increases compatibility between machines (Park column 1, lines 42-56).

31. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80386 Programming Techniques (herein referred to as Turley) in view of Hennessy and Patterson's Computer Architecture: A Quantitative Approach Second Edition (herein referred to as Hennessy). Turley has not taught wherein the native instructions are generated by compiling the non-native instruction. Hennessy has taught wherein the native instructions are generated by compiling the non-native instruction (Hennessy pages 89-96). A person of ordinary skill in the art at the time the invention was made would have recognized that a compiler allows various types of programming languages to be used and recognized on a single machine, thereby ensuring compatibility between various programs and the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to

incorporate the compiler of Hennessy in the device of Turley to ensure compatibility with various programs.

Response to Remarks

32. Applicant's arguments filed 21 July 2004 with respect to claims 1-51 in regards to Turley have been considered but are not considered persuasive. The claims describe elements within the segment descriptor and control register needed to determine a default address size, and that two operating mode indications and an enable are used to produce a default address size. However, there is no description about how the operating mode indications and enable indication interact, just a statement that interaction occurs. The details of the interaction, i.e. how the indications are explicitly used to define a default address size, are provided in the dependent claims, which have been objected to as being dependent on a rejected claim but containing allowable subject matter. Also, the claim language does not specify exactly what "address size" refers to, because "address size" could refer to the size of the address space or the number of bits needed to represent a valid address.

33. In order to clarify how Applicant's claims correspond to Turley, the examiner has mapped limitations of claim 1 to the device described in Turley with further explanation of the cited art.

Limitation in Question from Claim 1	**Corresponding Limitation in the Turley Reference for the Rejection of the Limitation**
A first storage location configured to store a segment selector	Turley states on page 63, paragraph 4, "An 16-bit value that you write into a segment register is called a *selector*". This indicates that a value stored in a segment register is a segment selector.
Identifying a segment descriptor including	Turley states on page 63, paragraph 4, "...because it [the segment selector] selects a segment descriptor". This indicates that the segment selector identifies a segment descriptor.
A first operating mode indication	Turley shows in the table "A segment descriptor" on page 49 that there are various parts to a segment descriptor, including the segment's privilege level, which the examiner considers to be the first operating mode indication. On pages 10, 46-47, and 51, Turley states that the descriptor privilege level (DPL) indicates whether the application can access certain parts of memory, including whether the segment of memory is accessible.

A second operating mode indication, and	Turley shows in Figure 2-2 on page 50 that there is a G bit in the segment descriptor and describes its function further on page 47, paragraph 3; page 52, G; and page 54, paragraphs 2-3. To summarize, the granularity (G) bit is used as the default for determining the address size represented by the limit field. The limit field indicates the maximum number of addressable values in the address space, and the G bit indicates whether the limit field is a factor of 1 byte or 4096 bytes. Further explanation is provided below in response to Applicant's arguments.
One or more bits identifying a segment described by said segment descriptor as a code segment;	Turley shows in Figure 2-2 on page 50 that there is a Type field in the segment descriptor and describes its function further on page 51, Type and pages 55-57. As clearly stated on page 51 in **Type**, the Type field indicates which type of segment is defined, one type of which is the code segment (Turley Page 52, Type).
A second storage location configured to store an enable indication,	Turley shows on page 26, Control Register 0, PE that indicates whether Real mode is enabled or Protected mode is enabled, which is needed to implement segmentation in the manner described, as stated in Turley on page 45 in paragraph 2 "Second there is the method of segmentation used in protected mode" and page 47 in paragraph 2 "...concept of a segment is very different on an 80386 system running in Protected mode".

Wherein said enable indication, said first operating mode indication, and said second operating mode indication are indicative of a default address size; and a processor configured to process an instruction using said default address size.	Applicant does not provide details in this claim on how the enable indication, first operating mode indication, and second operating mode indication interact to establish a default address size. Applicant has only claimed that these three indications are used in some undefined way to establish the default address size. The signals indicated above interact in the following manner to establish a default address size. First, the PE bit in Control Register 0 must be set to enable protected mode (Turley page 26, Control Register 0, PE) in order for segmentation to even be possible (Turley page 45, paragraph 2 "...the method of segmentation used in Protected mode" and page 47, paragraph 2 "...concept of a segment...running in Protected mode"). In essence, when the PE bit is not set, the segmentation described is disabled and, when the PE bit is set, the segmentation is enabled. Second, the DPL bit must match to allow access to the segment of memory. If access is not granted to the segment of memory, the segment cannot be accessed to set the address size. Finally, the G bit establishes the address size, since it is used as the default for determining the address size represented by the Limit field. The G bit indicates whether the address space size spans one megabyte (1MB) of space or up to four gigabytes (4GB) of space. Therefore, in order to establish a default address size, Protected mode must be enabled by the PE bit, the DPL bit must indicate that segment memory is accessible, and the G bit is accessed to establish the address size.

34. The following shows what the examiner considers equivalent limitations found in claim 1, which is the device claim of the apparatus, and in claim 23, which is the method claim of the same apparatus. The rejection used for the limitation in claim 1 explained in detail in the above table and in the response to arguments below applies to the equivalent limitation in claim 23.

Limitation in Claim 1 (The device claim)	**Equivalent Limitation in Claim 23 (The method claim)**
A segment register configured to store a segment selector	
Identifying a segment descriptor including	A segment descriptor
A first operating mode indication	A first operating mode indication in a segment descriptor, and
A second operating mode indication, and	A second operating mode indication in said segment descriptor,
One or more bits identifying a segment described by said segment descriptor as a code segment;	Wherein said segment descriptor further includes one or more bits that identify a segment described by said segment descriptor as a code segment;
A control register configured to store an enable indication,	An enable indication in a first storage location,

Wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication.	Determining a default address size in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor... and Generating addresses of said default address size.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

35. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
18 October 2004